REMARKS

Claims 27, 29, 30, 32, 33 and 35 have been amended. No claims have been added or cancelled. Therefore, claims 1-35 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Claim Objections:

Claims 27 and 32 have been amended to overcome the informalities objected to by the Examiner. Specifically, claim 27 has been amended to recite, "duplicates a trace in a trace cache," and claim 32 has been amended to recite, "searching a trace cache," as suggested by the Examiner. Other similar informalities have been addressed in amendments to claims 27, 29, 30, 32, 33 and 35.

Section 112, Second Paragraph, Rejection:

The Examiner rejected claim 28 under 35 U.S.C. § 112, second paragraph, as indefinite. Specifically, the Examiner submits that there is insufficient antecedent basis for the limitation "continuing construction of an incomplete trace already in progress" in this claim, as there is no mention of continuing construction of an incomplete trace in the specification. Applicants traverse this rejection for at least the following reasons.

Paragraph [0053] of the specification describes FIG. 4. This paragraph includes the following description:

> Block 351 shows an instruction being received. At 353, if a trace or traces duplicating the trace under construction and/or the next trace to be constructed have not been identified in the trace cache, the operations corresponding to the instruction may be used to fill vacant operation positions for a trace, as shown at 355. (emphasis added).

Applicants assert that this passage of the specification clearly describes that operations of the received instruction may be added to an incomplete trace (i.e., one

having vacant operation positions), thus "continuing its construction," as recited in claim 28.

Applicants remind the Examiner that the subject matter of a claim need not be described literally in order for the disclosure to satisfy the description requirement of §112. As repeatedly stated by the Board of Patent Appeals & Interferences and by the Court of Appeals for the Federal Circuit, it is well settled law that the invention claimed does not have to be described *in ipsis verbis* in order to satisfy the requirements of §112. *Jacobs v. Lawson*, 214 USPQ 907, 910 (B.P.A.I. 1982). When considered as a whole, the description and drawings in the application clearly support the above-referenced limitation of claim 28. Therefore, removal of the rejection of claim 28 is respectfully requested.

Section 102(b) Rejection:

The Examiner rejected claims 1, 2, 11-15, 24-26 and 32-34 under 35 U.S.C. § 102(b) as being anticipated by Rotenberg et al. (hereinafter "Rotenberg"). Applicants respectfully traverse this rejection for at least the following reasons.

Regarding claim 1, the Examiner asserts that Rotenberg teaches a prefetch unit coupled to the instruction cache, the branch prediction unit, and the trace cache in FIG. 4 and Section 2.2. The Examiner submits that Rotenberg's instruction latch appears to fill the role of Applicants' *prefetch unit*. However, Applicants assert that one of ordinary skill in the art could not reasonably consider a simple latch, as described in Rotenberg, to be the *prefetch unit* of the present invention, and this latch is not described as having any of the functionality of the *prefetch unit* recited in Applicants' claims.

For example, claim 1 recites, "if the prefetch unit identifies a match for the predicted target address in the trace cache..." Rotenberg's instruction latch clearly does not identify a match for a predicted target address in the trace cache, as it simply serves to latch the output of a 2:1 mux and does not even determine which of the inputs of the mux to latch (see FIG. 4). There is clearly nothing in Rotenberg that discloses this latch

performing a comparison of a predicted target address to addresses in the trace cache. Instead, logic within Rotenberg's trace cache itself (hit logic, FIG. 4) determines if there is a hit for a branch prediction.

In addition, claim 1 recites, *the prefetch unit is configured to fetch instructions from the instruction cache until the branch prediction unit outputs a predicted target address* and *if the prefetch unit identifies a match for the predicted target address in the trace cache, the prefetch unit is configured to fetch one or more of the plurality of traces from the trace cache.* Contrary to the Examiner's assertion, Rotenberg's instruction latch clearly does not perform these functions. The Examiner submits that Rotenberg teaches these limitations in Section 2.2, "on a trace cache miss, fetching proceeds normally from the instruction cache" and "on a trace cache hit, an entire trace of instructions is fed into the instruction latch, bypassing the instruction cache." However, as illustrated in FIG. 4, Rotenberg's core fetch unit, not the instruction latch, fetches instructions from the instruction cache (see, e.g., Section 2.1, paragraph 1-3) and outputs them to a 2:1 mux. In addition, Section 2.2, paragraph 3 states, "The trace cache is accessed in parallel with the instruction cache and BTB using the current fetch address." Thus, contrary to the limitations recited in Applicants' claim 1, instructions are always fetched from the instruction cache and the trace cache in parallel, and these two sets of instructions are output to the mux illustrated in FIG. 4. There is nothing in Rotenberg that discloses a prefetch unit that fetches instructions from an instruction cache until a branch prediction unit outputs a predicted target address and then fetches instructions from a trace cache instead. The fetching operation is not performed by Rotenberg's instruction latch, as the Examiner suggests, nor does it change when a predicted target address is output, as recited in Applicants' claim 1. Instead, the determination of whether there is a trace cache hit (performed in the trace cache itself) selects which inputs of the mux (instructions already fetched from the instruction cache or instructions already fetched from the trace cache) are fed to the instruction latch.

Finally, detecting a trace cache miss is clearly not the same as outputting a predicted target address, one for which a comparison to addresses in the trace cache has

not yet taken place. There is clearly nothing in Rotenberg to teach or suggest that a prefetch unit stops fetching from the instruction cache in response to a predicted target address merely being output, as recited in Applicants' claim 1.

Applicants remind the Examiner that anticipation requires the presence in a single prior art reference disclosure of each and every limitation of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For at least the reasons discussed above, Rotenberg clearly cannot be said to anticipate claim 1. Thus, the rejection of claim 1 is not supported by the cited art and removal thereof is respectfully requested.

Claim 14 includes limitations similar to claim 1, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 32, contrary to the Examiner's assertion, Rotenberg fails to teach or suggest *continuing to fetch instructions from the instruction cache until a branch target address is generated*. Again, the Examiner cites Section 2.2 "on a trace cache miss, fetching proceeds normally from the instruction cache" as teaching this limitation. However, as discussed above, there is nothing in Rotenberg that discloses fetching instructions from the instruction cache only until a branch target address is generated. Instead, FIG. 4 and its description clearly illustrate that instructions are continuously fetched from the instruction cache by the core fetch unit and that instructions are fetched from the trace cache in parallel, although the instructions fetched from the instruction cache may not be latched and passed to the decoder if the alternate input (from the trace cache) is selected at the 2:1 mux. Furthermore, detecting a trace cache miss is clearly not the same as generating a branch target address, one for which a comparison to addresses in the trace cache has not yet taken place. There is nothing in Rotenberg to teach or suggest that fetching from the instruction cache stops in response to a branch target address merely being generated, as recited in claim 32. In fact, claim 32 further recites,

"if a branch target address is generated, searching a trace cache for an entry corresponding to the branch target address." Therefore, in the claimed invention, the trace cache is not searched for a cache hit unless a branch target address is output, in which case the prefetch unit stops fetching instructions from the instruction cache. In Rotenberg, by contrast, the trace cache is accessed in parallel with the instruction cache and BTB (branch target buffer) using the current fetch address (see, e.g., Section 2.2, paragraph 3). There is nothing in Rotenberg that teaches or suggests that the trace cache is searched only if a branch target address is generated, as in Applicants' claim, and this paragraph teaches away from this limitation.

For at least the reasons above, Rotenberg clearly cannot be said to anticipate claim 32. Therefore, the removal of the rejection of claim 32 is respectfully requested.

Section 103(a) Rejections:

The Examiner rejected claims 3 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Patterson et al. (hereinafter "Patterson"), claims 4, 10, 17 and 23 as being unpatentable over Braught, claims 5-8 and 18-21 as being unpatentable over Rotenberg and Braught, and further in view of Lange et al. (U.S. Patent 3,896,419) (hereinafter "Lange"), claims 9 and 22 as being unpatentable over Rotenberg in view of Akkary et al. (U.S. Patent 6,247,121) (hereinafter "Akkary"), and claims 27-31 and 35 as being unpatentable over Rotenberg and Braught in view of Akkary. Applicants respectfully traverse these rejections for at least the following reasons.

Regarding claim 27, the Examiner submits that Rotenberg teaches *a method... comprising starting construction of a new trace if the received instruction is associated with a branch label* (Section 2.2, Rotenberg starts traces on branches, which branch to labels – or addresses, as shown by Braught), but fails to teach *receiving a retired instruction*. The Examiner admits that Rotenberg does not teach that instructions need to be retired before the trace can be generated and relies on Akkary to teach this limitation. The Examiner submits that Akkary teaches that instructions are not put into the trace

buffers until they have been retired, to ensure that they executed correctly (column 3, lines 40-44). This passage includes the following description:

> Final retirement logic 134 finally retires instructions in trace buffers 114 after it is assured that the instructions were correctly executed either originally or in re-execution.

The Examiner has incorrectly interpreted this passage as teaching that instructions are not put into the trace buffers until they have been retired. **This passage actually says just the opposite**, that is, that instructions placed in the trace buffer stay in the trace buffer until they are retired. This is clear from the following two passages (emphasis added):

> column 6, lines 53-56:
>
> all needed details regarding the instruction are maintained in trace buffers 114 and MOB 178 until a final retirement, described below.

> column 10, lines 1-10:
>
> In one embodiment of the invention, final retirement includes... (3) deallocation of trace buffer and MOB 178 resource entries.

Therefore, Rotenberg and Braught in view of Akkary clearly fails to teach or suggest this limitation of Applicants' claim 27.

The Examiner also admits that Rotenberg fails to teach *if a previous trace under construction duplicates a trace in a trace cache, delaying construction of the new trace until the received instruction corresponds to a branch label.* The Examiner cites Lange in his arguments regarding these limitations. **However, claim 27 was rejected as being unpatentable over Rotenberg and Braught in view of Akkary, not Lange. Therefore, the Examiner's remarks are improper.**

Furthermore, the Examiner submits that Lange teaches a system in which a cache is checked for a match with memory, while the memory is being read at the same time, with the advantage that there is no delay in the overall data fetch cycle if there is no match in the cache, and the memory access can be cancelled before it incurs any system

slowdown as well (column 2, lines 13-31, and column 5, lines 5-10). Given this advantage, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to check the trace cache for a duplicate copy of the trace at the same time the trace was being constructed, in order to minimize or eliminate delay in generating the trace in the case that the trace is not in the cache, and aborting the unnecessary trace if it is found in the cache. The Examiner further asserts that when a trace is found to be in the cache, and the trace generation is aborted, it is obvious that a new trace would not be built until a new branch (which would have to be associated with a branch label) was retired. **The Examiner's reasoning is clearly flawed.** First, claim 27 does not recite fetching data from memory or with checking for a cache hit on a memory access. Instead, this claim describes construction of a trace from retired (e.g., completed) instructions. The construction of a trace from retired instructions does not require fetching data from memory and, thus, the issue suggested by the Examiner (delay in generating the trace in the case that the trace is not in the cache) would not exist. The Examiner seems to suggest that generating a trace in a trace cache necessarily results in a system slowdown, providing motivation to avoid construction of duplicate traces. However, the Examiner has not provided any evidence that this is the case.

Applicants remind the Examiner that to establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond,* 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). As discussed above, the cited art does not teach or suggest all limitations of claim 27, nor do they include any suggestion or incentive to modify their teachings to produce the claimed invention.

For at least the reasons above, the rejection of claim 27 is not supported by the cited art and removal thereof is respectfully requested.

Claim 35 includes limitations similar to claim 27, and so the arguments presented above apply with equal force to this claim, as well.

Applicant also asserts that the rejection of numerous ones of the dependent claims is further unsupported by the cited art. However, since the rejection has been shown to be unsupported for the independent claims, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-88700/RCK.

Also enclosed herewith are the following items:

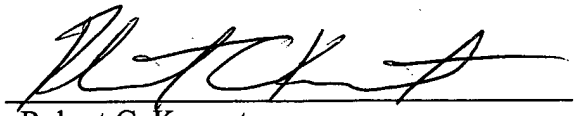
☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Other:

Respectfully submitted,



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